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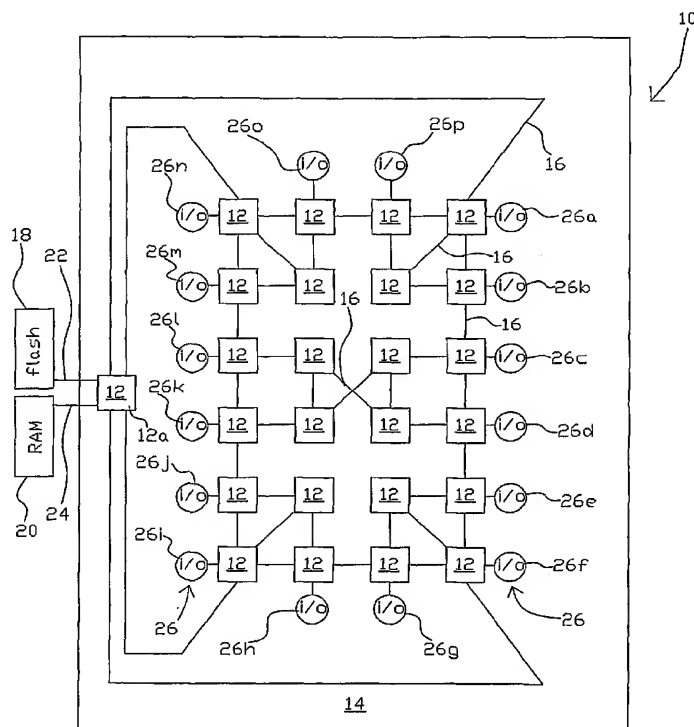
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[Continued on next page]

(54) Title: COMPUTER PROCESSOR ARRAY



(57) Abstract: A computer array (10) has a plurality of computers (12) for accomplishing a larger task that is divided into smaller tasks, each of the smaller tasks being assigned to one or more of the computers (12). Each of the computers (12) may be configured for specific functions and individual input/output circuits (26) associated with exterior computers (12) are specifically adapted for particular input/output functions. An example of 25 Computers (12) arranged in the computer array (10) has a centralized computational core (34) with the computers (12) nearer the edge of the die (14) being configured for input and/or output.



SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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COMPUTER PROCESSOR ARRAY

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the field of computers and computer processors, and more particularly to a method and means for connecting computers together such that the overall speed and efficiency of the combined computers is optimized. The predominant current usage of the present inventive computer array is in the combination of multiple computers on a single microchip, wherein cooperation of the computers to achieve a unified object is desirable.

15

Description of the Background Art

In the art of computing, processing speed is a much desired quality, and the quest to create faster computers and processors is ongoing. Since, for any given state of the art, the maximum available processor speed is finite, there have been efforts to use multiple processors or multiple computers to speed up operations. It is known in the art to combine a plurality of computer processors or computers to divide a task or computation, such that the task is achieved in a minimum amount of time. An example is a multi-threading application wherein different program threads are operated upon by different processors.

As discussed above, it is a given that it is desirable to speed up the operation of a computer process. However no prior art method or apparatus has achieved an optimal speed for the performance of many computer operations.

25

SUMMARY

Accordingly, it is an object of the present invention to provide an apparatus and method for increasing computer processing speed.

5 It is still another object of the present invention to provide an apparatus and method for providing substantial computing power inexpensively.

It is yet another object of the present invention to provide an apparatus and method for increasing the operational speed of a multi-computer array.

10 It is still another object of the present invention to provide an apparatus and method for accomplishing computational intensive tasks.

Briefly, a known embodiment of the present invention is an array of computers, each computer having its own memory and being capable of independent computational functions.

A task, such as the implementation of a digital radio, a digital stereo preamplifier, a Global Positioning System ("GPS") receiver unit, a radio transceiver, a speech recognition device, or
15 any of many other such functions, is divided into a plurality of sub-operations, and each operation is assigned to one of the computers at initiation of the operation of the array.

In the embodiment of the invention described, the computer array is implemented on a single die, with at least some computers near the edge of the die being configured to accomplish input and output tasks. Connections between the computers are arranged to keep
20 the implementation of the device relatively simple, while minimizing the number of "hops" required to communicate across the array. In a described embodiment, the computers are arranged in a 5 by 5 matrix wherein each of the computers connects directly to three of its neighbor computers by a parallel connection, although other types and quantities of connections are within the scope of the invention.

25 The inventor has found that, although assigning a separate task initially to each of the computers may result in some idle time for some or all of the computers, the lack of complexity and inherent efficiency of the arrangement will more than make up for any inefficiency caused by such idle time, and the overall speed and ease of the accomplishment of the task is greatly enhanced.

30 These and other objects and advantages of the present invention will become clear to those skilled in the art in view of the description of modes of carrying out the invention, and the industrial applicability thereof, as described herein and as illustrated in the several figures

of the drawing. The objects and advantages listed are not an exhaustive list of all possible advantages of the invention. Moreover, it will be possible to practice the invention even where one or more of the intended objects and/or advantages might be absent or not required in the application.

5 Further, those skilled in the art will recognize that various embodiments of the present invention may achieve one or more, but not necessarily all, of the described objects and/or advantages. Accordingly, the objects and/or advantages described herein are not essential elements of the present invention, and should not be construed as limitations.

10 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic view of a computer array, according to the present invention;

Fig. 2 is a block diagrammatic view of an example of one of the computers of Fig. 1;

15 Fig. 3 is a diagrammatic view of a computer array configured for a specific application, according to the present invention; and

Fig. 4 is a flow diagram depicting an example of the present inventive method.

20 DETAILED DESCRIPTION OF THE INVENTION

This invention is described in the following description with reference to the Figures, in which like numbers represent the same or similar elements. While this invention is described in terms of modes for achieving this invention's objectives, it will be appreciated by
25 those skilled in the art that variations may be accomplished in view of these teachings without deviating from the spirit or scope of the present invention. The method form of the invention may be practiced by combining one or more machine readable storage devices containing the code, according to the present invention, with appropriate standard computer hardware to execute the code contained therein.

30 The embodiments and variations of the invention described herein, and/or shown in the drawings, are presented by way of example only and are not limiting as to the scope of the invention. Unless otherwise specifically stated, individual aspects and components of the

invention may be omitted or modified, or may have substituted therefore known equivalents, or as yet unknown substitutes such as may be developed in the future or such as may be found to be acceptable substitutes in the future. The invention may also be modified for a variety of applications while remaining within the spirit and scope of the claimed invention, since the range of potential applications is great, and since it is intended that the present invention be adaptable to many such variations.

A known mode for carrying out the invention is an array of individual computers. The inventive computer array is depicted in a diagrammatic view in Fig. 1 and is designated therein by the general reference character 10. The computer array 10 has a plurality (twenty five in the example shown) of computers 12. In the example shown, all of the computers 12 are located on a single die 14. According to the present invention, each of the computers 12 is a generally independently functioning computer, as will be discussed in more detail hereinafter. The computers 12 are interconnected by a plurality (the quantities of which will be discussed in more detail hereinafter) of interconnecting data lines 16. In this example, the data lines 16 are asynchronous high speed parallel data lines, although it is within the scope of the invention that other interconnecting means (such as serial data lines) might be employed for the purpose. In the present embodiment of the array 10, not only is data communication between the computers 12 asynchronous, the individual computers 12 also operate in an asynchronous mode. While this is not a necessary aspect of the invention, it is thought by the inventor to provide important advantages. For example, since a clock signal does not have to be distributed throughout the computer array 12, a great deal of power is saved, and one skilled in the art will know that this is an important advantage. Furthermore, not having to distribute a clock signal eliminates many timing problems that could limit the size of the array 12 or cause other known difficulties.

It should be noted that the view of Fig. 1 is not intended to be a layout diagram of the computers 12. Rather, this view illustrates an example of possible interconnections of the computers 12. In the view of Fig. 1 it can be seen that adjacent examples of the computers 12 are connected to three of the neighbor computers 12 by three of the data lines 16. It is thought by the inventor that this quantity of data lines 16 is a reasonable quantity, since it minimizes the necessary quantity of metal layers on the die 14, while providing sufficient data paths that a minimum number of "hops" is required to communicate from one of the computers 12 on the perimeter of the array 10 to even the most interior computer 12, where

the term "hops" is used to mean the connections or transfers between the computers 12 through which a signal must travel to move from one of the computers 12 to another computer 12.

Also pictured in the view of Fig. 1 are a flash memory 18 and a RAM 20. In the embodiment shown, the flash memory 18 and the RAM 20 are "off chip", meaning that they are not on the die 14, although it is within the scope of the invention that one or both of these might conceivably be located on the die 14. The flash memory 18 is used to load initial programs into the computers 12 at power up, and the RAM 20 is used in the conventional manner. A memory controller computer 12a controls access to memory in the flash memory 18 and the RAM 20. In the embodiment of the invention described, the flash memory 18 uses a serial data line 22 to transfer data to and through the memory controller computer 12a, while the RAM 20 utilizes a parallel data bus 24, because it is desirable to have as fast as possible a connection to the RAM 20.

The example of the memory controller computer 12a serves to illustrate an important aspect of the present invention. While, according to the present invention, the several computers 12 are either exactly or essentially alike, they each can be configured to perform very distinct and different functions. It should be noted that, according to the present invention, the computers 12 are essentially identical computers in that the structure, circuitry, layout, and operational characteristics are essentially the same. Some examples of minor differences that may be optionally provided will be discussed herein. However, it remains true that the arrays 10, 10a of the present invention are arrays of computers 12 that are all essentially the same. In other words, the present arrays 10, 10a are homogeneous arrays rather than heterogeneous arrays of computers which are designed from the outset to perform different functions. Although the computers 12 of the present homogeneous arrays 10, 10a are all essentially the same, they can be adapted for special purposes by the addition of a small amount of additional circuitry, as will be discussed in more detail hereinafter. Among the many advantages of the homogeneous arrays of the present invention is versatility. According to the present invention, the arrays 10, 10a can be used for a great many different purposes. Further, even if some modification is required or desirable for some special purpose, such modification can be easily accomplished during the manufacture of the devices.

The memory controller computer 12a is just one such example of one of the computers 12 performing a dedicated function. As can be seen in the example of Fig. 1, it is expected

that it might be beneficial for the memory controller computer 12a to have a greater quantity of the data lines 16 to connect it to the remainder of the computers 12 than just the quantity of three, previously discussed.

As discussed briefly above, many of the computers 12 in the computer array 10 will have different functions. Accordingly, it is thought that it will be most beneficial for the computers 12 nearest the edge of the die 14 to have input/output functions, since it will be easier to connect to the required pins from those external computers 12 if they are placed on the edge of the die 14. The interior computers 12 (those which are not on the outside of the computer array 10) will, therefore, be used more to accomplish computational and control functions, or other functions which typically require less input/output capability. In the view of Fig. 1, a plurality of input/output circuits 26 are associated with the corresponding computers 12, and provide the input/output functions, which will be discussed in more detail in an example hereinafter. Since the various input/output circuits 26 might each differ, according to their intended respective functions, they are designated by the differentiating designations 26a through 26p inclusive.

Fig. 2 is a block diagrammatic view of an example of one of the computers 12 of Fig. 1. As can be seen in the view of Fig. 2, the computer 12 has a processor 28, a ROM 30 and a RAM 32. As discussed previously herein, the computer 12 is, therefore, capable of performing its assigned function generally independently from all of the other computers 12 in the computer array 10 (Fig. 1).

Fig. 3 is a diagrammatic representation of an example of a computer array 10a showing one possible allocation of the computers 12 therein. The example of the computer array 10a of Fig. 3 differs from the first example of the computer array 10 of Fig. 1 in the allocation of the computers 12, as will be discussed in more detail hereinafter. It should be noted that, as with the view of Fig. 1, the view of Fig. 3 is not intended as a layout diagram and, therefore, is not intended to indicate a necessary physical placement of any of the computers 12. Nevertheless, the example of Fig. 3 is indicative of the fact that it is thought that the 5 by 5 computer array 10a is a useful physical arrangement of the computers 12. According to this arrangement there are sufficiently few computers that not too many are buried deep within the computer array 10a, such that more than a few "hops" would be required to relay data from one of the exterior computers 12, through others of the computers 12, to an interior computer 12. Further, the quantity of twenty five computers is well suited to maximize the usage of

available space on the die 14. It is anticipated that, even in many applications where all twenty five of the computers 12 are not required, it may well be cost efficient to use an array such as the example here described. It should be noted that the 5 by 5 arrangement of the computer array 10a and the quantity of twenty five of the computers 12, while thought to be a useful arrangement and quantity (as discussed above), is by no means thought to be the only useful arrangement and quantity. Presently, a 6 by 4 matrix having 24 of the computers 12 in the matrix, as discussed previously in relation to Fig. 1, is thought to have some particular advantages. For example, in an array wherein there are even numbers of the computers 12, the array can be made up of a plurality of 2 by 2 blocks of the computers. In such case, each of the computers 12 can be made to be a mirror image of the computers across from it in the block. This might make easier the task of computer design and interconnection layout. Indeed, factors to be discussed in more detail hereinafter dictate that essentially any quantity, from as few as four, up to and including literally thousands of the computers, could be arrayed together according to the present invention. Also, although the example of Fig. 1 shows three of the data lines 16 connecting each of the computers 12 to its neighbors, the inventor believes that another useful arrangement would be to have data lines 16 connecting each of the computers 12 to all of its nearest neighbor computers 12. In such a connection arrangement, the number of data lines 16 connected to each of the computer 12 would vary according to the placement of each computer 12 in the array10, 10a.

The example computer array 10a of Fig. 3 has the computers 12 assigned to tasks such as might be useful to create a global positioning system ("GPS") receiver. This example of Fig. 3 is presented only as an example of how various tasks might be assigned to the various computers 12. Interconnections are not shown, as they will not be substantially different from the example of Fig. 1, except as might be necessary or desirable to accomplish the specific tasks described.

In the example of Fig. 3 it can be seen that the computer array 10a has a computational core 34 which includes computers 12q through 12v, inclusive. The peripheral computers, 12a through 12p, are configured generally for input and output, as will be described in more detail hereinafter. Note that in the diagrammatic example of Fig. 3 the input/output circuits 26 which were shown separately in Fig. 1 are not shown separately. This is an example of the fact that the input/output circuits 26 may be considered to be variations in the individual computers 12a through 12w. Whether the input/output circuits 26 are shown separately or are

included as a part of the variations between the generally similar computers 12a through 12w is merely a difference in the manner of diagrammatic presentation.

In the example of Fig. 3, computer 12i is configured to be a RAM input/output device, while computer 12j is configured to be a flash memory input/output device. By a comparison to the example of Fig. 1, it can be seen that this example shows a variation in that the computer array 10 of Fig. 1 has a single computer 12 for handling the input and output from both the flash memory 18 and the RAM 20 (Fig. 1), while the present example of the computer array 10a divides these tasks between computers 12. Such a variation is typical of many such variations that might be applied to the computer array 10, 10a.

Returning to a discussion of the peripheral computers 12a through 12p, the computers 12a through 12d are configured for input and output to external devices. In the example shown, computers 12a through 12d implement a LAN interface, a USB interface, a Firewire interface, and a wireless interface, respectively. One skilled in the art will be familiar with the pin out and hardware protocols necessary to implement each of these functions in the computers 12a through 12d. Alternatively, one of the computers 12a through 12d could be used to implement a video output. In some applications fewer than the four input/output computers 12a through 12d might be required. For example, in some applications, only a USB interface might be sufficient input/output to external devices.

In the GPS receiver example of Fig. 3, the computer 12e provides a hardware control (which is a digital input and output) for setting parameters of the remainder of the receiver (not shown) external to the computer array 10a. The computer 12f provides hardware monitoring (which is an analog input and output) for monitoring parameters of operational aspects of the receiver. The hardware monitoring and control allows the computer array 10a to determine how well the rest of the GPS receiver is operating, as well as providing a means to set or modify various operating configurations of the rest of the receiver external to the computer array 10a.

Computers 12o and 12p are configured and programmed to sample and process received RF signals (analog to digital conversion) and the computer 12n is configured and programmed to provide reference frequencies for frequency down conversion prior to sampling (digital to analog conversion). Computer 12w and 12x are configured and programmed to decode the forward error corrected ("FEC") bit stream from the GPS signal. The FEC used in GPS signals will be familiar to one skilled in the art of GPS receivers.

Computer 12y and 12h are optionally used for decrypting aspects of the GPS bit stream after reception demodulation. Note that the use of computers 12y and 12h as described is optional because encryption and decryption will not normally be required in a GPS receiver. Although some parts of a GPS signal are encrypted, a commercial receiver will generally not have access to those. However, encryption will be required in a military version of a GPS receiver. Computer 12l is configured and programmed to communicate with additional computer array(s) 10, as may be necessary or desirable.

In the example of the computer array 10a of Fig. 3, computers 12 not specifically discussed above will either be spares (not used), or else could optionally be used to provide additional input and/or output functions and/or redundancy for the other computers 12.

Fig. 4 is a flow diagram depicting an example of an inventive computer array method 36, which will be understood in light of the preceding discussion of the computer array 10, 10a. In a "provide interconnected computers" 38 operation, the computers 12 described previously herein are provided in the computer array 10 with the interconnecting data lines 16. In a "configure computers for tasks" 40 operation, the provided computers 12 are provided with the distinctive data lines 16 and any other features which might be required to adapt the computer array 10 to a particular application. Of course, the preceding operations 38 and 40 will be accomplished prior to and during the manufacture of the computer array 10.

In an "assign tasks to computers" 42 operation, it is decided what portions of a particular task are best accomplished by which of the computers 12, and a program is written to assign and accomplish such tasks. When the computer array 10 is to be used, in an "initialize computers" 44 operation, the individual tasks are loaded into the computer RAM 32 of the computer 12 and operation is begun.

One skilled in the art will recognize that the listed operations of the computer array method 36 are not an exhaustive list of operations which will be used in conjunction with the manufacture and operation of the computer array 10, 10a. As just one example, one skilled in the art will recognize that, upon initialization of the computer array 10, 10a, a test routine will be run.

Various modifications may be made to the invention without altering its value or scope. For example, other quantities or arrangements of the computers 12 than those specifically discussed herein would be entirely within the spirit and scope of the invention. While specific examples of the arrangement and use of the computers 12 have been discussed

herein, it is expected that there will be a great many applications for the inventive computer array 10 which have not yet been envisioned. Indeed, it is one of the advantages of the present invention that the inventive method and apparatus may be adapted to a great variety of uses.

5 All of the above are only some of the examples of available embodiments of the present invention. Those skilled in the art will readily observe that numerous other modifications and alterations may be made without departing from the spirit and scope of the invention. Accordingly, the disclosure herein is not intended as limiting and the appended claims are to be interpreted as encompassing the entire scope of the invention.

10 INDUSTRIAL APPLICABILITY

The inventive computer array 10, 10a and associated method are intended to be widely used in a great variety of computer applications. It is expected that it they will be particularly useful in computer intensive applications wherein a great number of different but related
15 functions need to be accomplished. It is expected that some of the best applications for the inventive computer array 10, 10a, and associated method, will be where the needed tasks can be divided such that each of the computers 12 has computational requirements which are nearly equal to that of the others. However, even where some of the computers 12 might sometimes, or even always, be working at far less than their maximum capabilities, the
20 inventor has found that the overall efficiency and speed of the computer array 10, 10a will generally exceed that of prior art computer arrays wherein tasks might be assigned dynamically.

It should be noted that there might be many applications wherein it would be advantageous to have more than one of the computer arrays 10, 10a. One of many such
25 possible examples would be where a digital radio might require a GPS input. In such an example the radio might be implemented by one computer array 10, which receives input from a separate computer array 10 configured to accomplish the function of a GPS.

It should further be noted that, although the computers 12 may be optimized to do an individual task, as discussed in the examples above, if that task is not needed in a particular
30 application, the computers 12 can easily be programmed to perform some other task, as might be limited only by the imagination of the programmer.

It is anticipated that the present inventive computer array 10, 10a will best be

implemented using the Forth computer language, which is inherently segmented to readily divide tasks as required to implement the invention. Color Forth is a recent variation of the Forth language which would be equally applicable.

Since the computer array 10, 10a and computer array method 36 of the present invention may be readily produced and integrated with existing tasks, input/output devices, and the like, and since the advantages as described herein are provided, it is expected that they will be readily accepted in the industry. For these and other reasons, it is expected that the utility and industrial applicability of the invention will be both significant in scope and long-lasting in duration.

I CLAIM:

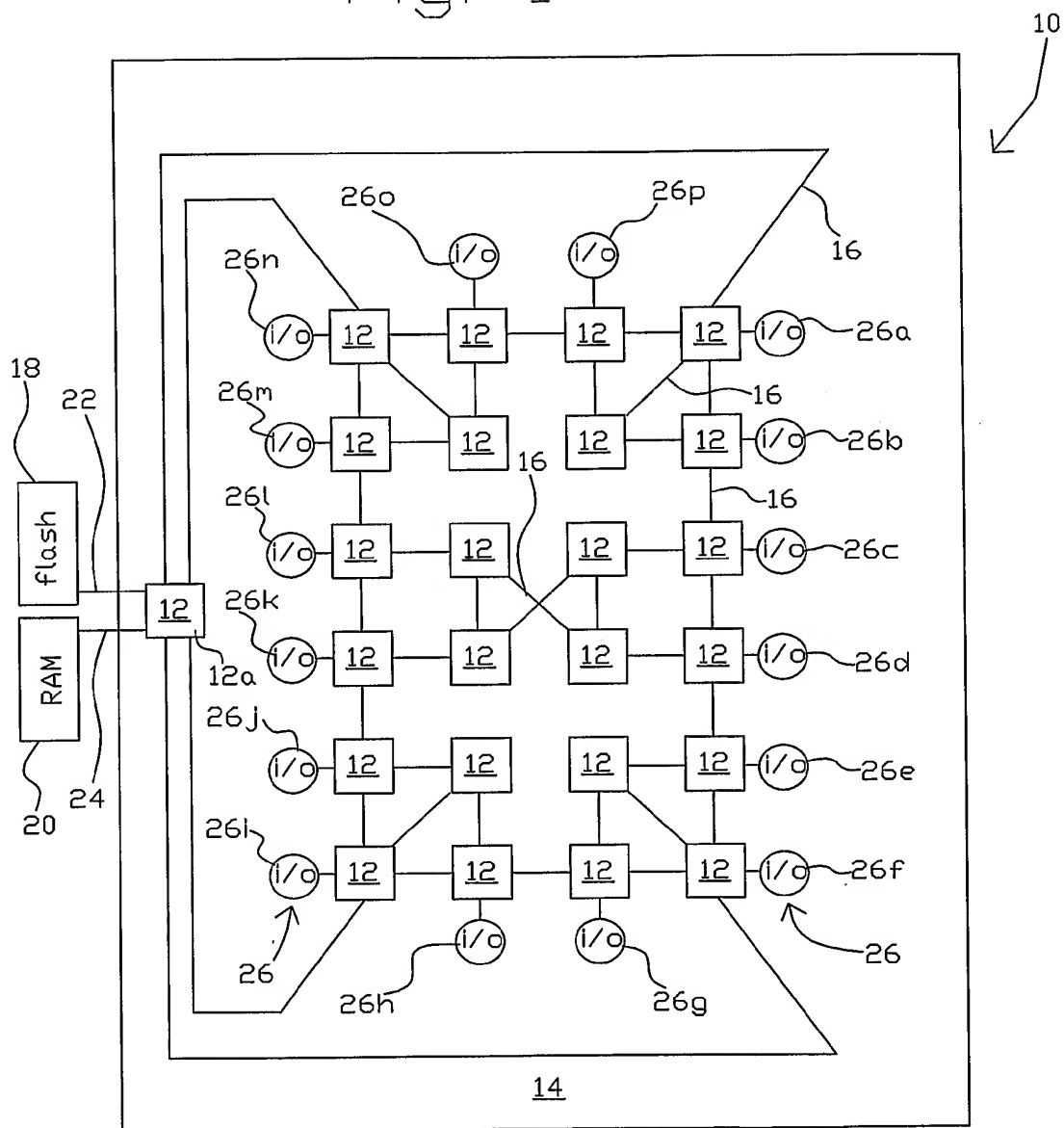
1. A computer array, comprising:
a plurality of computers;
and a plurality of data paths connecting the computers; wherein:
at least some of the computers are assigned a task different from that assigned to the other computers.
2. The computer array of claim 1, wherein:
each of the computers is assigned a task different from that of the other computers.
3. The computer array of claim 1, wherein:
at least some of the computers are configured for specific input functions.
4. The computer array of claim 1, wherein:
at least some of the computers are configured for specific output functions.
5. The computer array of claim 1, wherein:
communication between the computers is asynchronous.
6. The computer array of claim 1, wherein:
communication between the computers is via a plurality of parallel data lines.
7. The computer array of claim 1, wherein:
each of the computers is hard wired to communicate with at least three of the plurality of computers.
8. The computer array of claim 1, wherein:
the quantity of computers is 25.
9. The computer array of claim 1, wherein:
the computers are physically arrayed in a 5 by 5 array.

10. The computer array of claim 1, wherein:
at least some of the computers are physically arrayed in a 4 by 6 array.
11. The computer array of claim 1, wherein:
the quantity of computers along each side of the array is an even number.
12. The computer array of claim 1, wherein:
at least one of the computers is in direct communication with an external memory source.
13. The computer array of claim 1, wherein:
at least one of the computers communicates data from an external memory source to at least some of the plurality of computers.
14. A method for performing a computerized job, comprising:
providing a plurality of computers; and
assigning a different task to at least some of the computers.
15. The method of claim 14, wherein:
at least one of the computers is assigned to communicate with a flash memory.
16. The method of claim 14, wherein:
at least one of the computers is assigned to communicate with a random access memory.
17. The method of claim 14, wherein:
at least one of the computers is assigned to accomplish an input/output function.
18. The method of claim 14, wherein:
one of the computers routes assignments to the remainder of the computers.

19. A computer array, comprising:
a plurality of computers; and
a plurality of data connections between the computers; wherein
at least some of the computers are programmed to perform different functions.
20. The computer array of claim 19, wherein:
the different functions work together to accomplish a task.
21. The computer array of claim 19, wherein:
each of the functions is programmed into the respective computers when the computer array is initialized.
22. The computer array of claim 19, wherein:
communication between the computers is asynchronous.
23. A method for accomplishing a task using a plurality of computers, comprising:
dividing a task into operational components and assigning each of the operational components to one of the computers;
programming at least some of the computers to accomplish each of the operational components.
24. The method for accomplishing a task of claim 23, wherein:
the operational components are operations used in accomplishing a global positioning system receiver.
25. The method for accomplishing a task of claim 23, wherein:
before the task is begun, programming the computers to accomplish each of the operational components.
26. The method for accomplishing a task of claim 23, wherein:
the computers are arranged in a computer array.

1/3

Fig. 1



2/3

Fig. 2

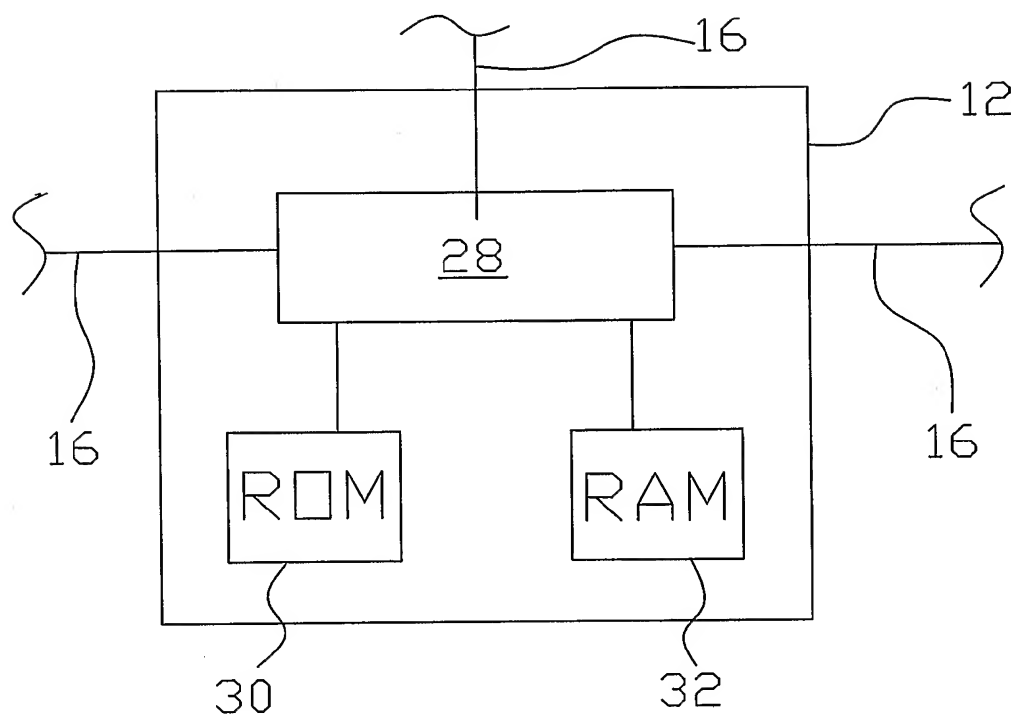


Fig. 4

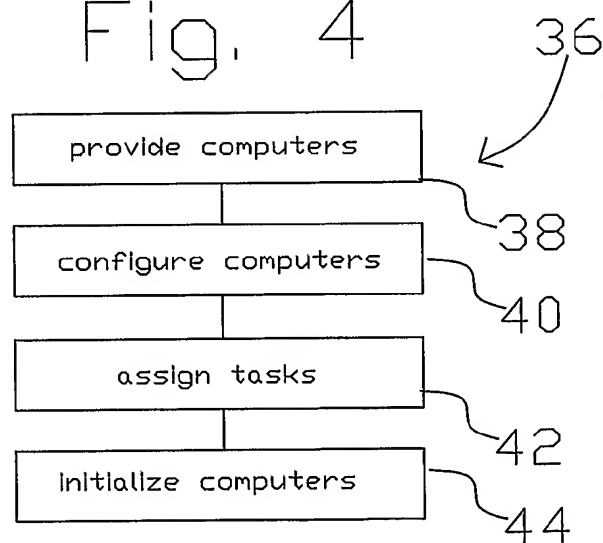


Fig. 3

